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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,946	07/10/2001	Fumio Hirahara	211134US2S	7965

22850 7590 10/16/2002

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EXAMINER
MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/900,946	Applicant(s) HIRAHARA ET AL.	
	Examiner James Mitchell	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> ((b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 6-8, 10-13, 15-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuda (EP 0588094).

3. Matsuda discloses (Fig 1; Column 6, Lines 2-6) a plurality of semiconductor chips comprising a transistor (29) that inherently comprises an insulation layer and a diode (31), at lease three power terminals (3,5,7) superimposed on each other, and at least one semiconductor chip sandwiched between a predetermined said two terminals in a device for large power (Column 1, Lines 5-7), wherein a portion of a terminal (defined by the top portion of the terminals 3 & 5) on one end among superposed power terminals of a power terminal and a power terminal on the other end among said superposed power terminals are led out in the same direction (3,5), wherein the middle terminal (5, via the top portion) is led out in a direction opposite to a power terminal (7), with at least a first and second face of said semiconductor chip connected to a first and second power terminal through soldering (Column 6, Lines 3-6; via both the chip and terminals being attached to substrate,15), and a control electrode (17) and electrode pad (inherent pad formed on chip) connected by wirebonding (Column 6, Lines 32-35); and at least one chip interposed between a predetermined two power terminals (Fig 2) and

inherently electrically connected to the two power terminals (Abstract) by soldering (Column 6, Lines 4-6); wherein a portion of the uppermost one and lowermost one of said at least three power terminals extend in a same direction; a chip interposed between said terminals includes a plurality of semiconductor chips (29, 31); said transistor inherently has a control electrode (via gate electrode) to control said at least one transistor; said control pad is inherent in wirebond and is inherently connected to the control electrode to control at least one transistor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 5, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda.

7. Matsuda discloses elements stated in paragraph 3 and a screw fixing structure (Fig 3, Item 59).

8. Although Matsuda does not appear to explicitly teach "two current flow in opposite directions in said uppermost and lowermost one of the said terminals" and having a screw structure "so as to connect said at least one semiconductor chip by pressure welding", this statement of intended use does not result in a structural difference between the claimed apparatus and the apparatus of Matsuda. Further, because the apparatus of Matsuda is inherently capable of being used for the intended use the statement of intended use does not patentably distinguish the claimed apparatus from the apparatus of Matsuda. Similarly, the manner in which an apparatus operates is not germane to the issue of patentability of the apparatus; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is,

not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

9. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda.

10. Matsuda discloses elements stated in paragraph 3, but does not appear to disclose that the control electrode is led out in a direction opposite or perpendicular to said at least one power terminal.

11. In any case, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Response to Arguments

12. Applicant's arguments filed July 23. 2002 have been fully considered but they are not persuasive. Applicant contends that the power terminals are adjacent and parallel

and not above one another as claimed. First, Examiner respectively directs applicant to the meaning of adjacent, which is defined in Webster's dictionary as "nearby". The two words are not mutually exclusive. Secondly, applicant's basis for his position can only be drawn from the figures in the prior art, which are only illustrative (emphasis added). A semiconductor device can be mounted in its final structure along any axis (E.G. X, Y, Z –axis). The drawing only shows the device along the X-axis, however the package can be mounted along the Y-axis, wherein one terminal would be "higher" than the other terminal and therefore "above." Since one terminal would be higher, it satisfies the claim limitation of "above".

13. Applicant's second notion that the chip's upper and lower surfaces are not connected to two power terminals is incorrect. Applicant correctly states (Page 6) that in Matsuda, the chips are on top of the second conductor, but fails to state that the first power terminal is connected to the second conductor and therefore connected to the bottom of said chips. Further, applicant correctly, states that the upper surface of the chips are wire bonded to a third conductor, but fails to indicate that a second conductor is fixed on the third conductor and therefore connected to the upper surface of the chips. The broad limitation of claim 1 has been met.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmm
October 7, 2002

DAVID L. TALBOTT
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800